REMARKS

Claims 1-62 are pending. Claims 1, 15, 29, 43, 57, and 60 are in independent form.

In the action mailed February 8, 2007, claims 58-62 were recognized as reciting allowable subject matter. Applicant acknowledges the recognition of allowable subject matter with appreciation.

Claim 1 was rejected under 35 U.S.C. § 101 as allegedly being directed to a judicial exception to the statutory subject matter defined in 35 U.S.C. § 101. In particular, the rejection of claim 1 contends that making useful parameters available is not a tangible result because it is not clear whether the parameters will "actually be used" for a described utility.

Applicant respectfully disagrees. Intermediates have long been recognized as deriving their utility from a *potential* use in generating final products of known utility. *See, e.g., M.P.E.P.* § 2107.01 (describing that intermediates lack a utility only when a final product has no utility). In the claim 1, since the final product of management of the display buffer has a specific, substantial, and credible utility, the making of buffer management parameters suitable for management of the display buffer available also has utility. Accordingly, the rejection of claim 1 under 35 U.S.C. § 101 is improper and applicant asks that it be withdrawn.

Claim 29 was rejected under 35 U.S.C. § 101 as allegedly being directed to a judicial exception to the statutory subject matter defined in 35 U.S.C. § 101. In particular, the rejection of claim 29 appears to contend that an "article comprising a storage medium" is not patentable subject matter but a "computer program product that comprises a computer readable medium" is patentable subject matter. The alleged basis for this distinction is that an article "could be taken to be an entity that is completely separate from a computer and simply stores the instructions without the computer reading the instruction[s] and executing those instructions."

Applicant respectfully disagrees with the rejection on several bases. To begin with, 35 U.S.C. § 101 does not preclude entities that are "completely separate from a computer" from patentability. Indeed, much of 35 U.S.C. § 101 was written before the invention of many computers. It would border on the absurd for the legislature to have drafted a law precluding articles from patentability if they were "completely separate" from devices that had not yet been invented.

Moreover, there is no basis for the contention that articles which store instructions without a computer reading the instructions are not patentable subject matter. For example, M.P.E.P. § 2106.01 states that:

> "a claimed computer-readable medium encoded with a computer program is a computer element which defines structural and functional interrelationships between the computer program and the rest of the computer which permit the computer program's functionality to be realized, and is thus statutory. *See M.P.E.P.* § 2106.01 (*citing In re Lowry*, 32 F.3d 1579, 1583-84 (Fed. Cir. 1994).

Note that there is no requirement that a computer read a computer program encoded on a computer-readable medium set forth in the M.P.E.P. Instead, a computer-readable medium encoded with a computer program defines structural and functional interrelationships and hence constitutes patentable subject matter. Since claim 29 recites "an article [that comprises] a storage medium which stores computer-executable instructions, the instructions being readable and operable to cause a computer to perform operations," claim 29 is statutory. Accordingly, the rejection of claim 29 under 35 U.S.C. § 101 is improper and applicant asks that it be withdrawn.

CLAIMS 1 AND 29

Claims 1 and 29 were rejected under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 5,953,020 to Wang et al. (hereinafter "Wang") and U.S. Patent No. 6,499,072 to Frank et al. (hereinafter "Frank").

Claim 1 relates to a method of determining buffer management information for a data processing system. The method includes determining a latency parameter based on a first system configuration of the data processing system, determining a buffer drain rate based on a first display mode of the data processing system, calculating one or more buffer management parameters based on at least the latency parameter and the buffer drain rate, and making the one or more buffer management parameters available for management of the display buffer. The latency parameter represents a latency time amount between a display data request and delivery of display data to a display buffer.

Claim 29 relates to an article that includes a storage medium which stores computer-executable instructions. The instructions are readable and operable to cause a computer to perform operations that include activities corresponding to those of claim 1.

The rejections of claims 1 and 29 are based on the contention that Frank's data issue delay data 24 constitutes a latency parameter. In particular, the rejection contends that "the latency time amount between a display data request and delivery of display data to a display buffer is essentially the amount of time it takes for the display engine to access the memory to obtain display data."

This is simply not true. Indeed, Frank himself provides support for the opposite conclusion. In this regard, as discussed in the response filed November 28, 2006, Frank's data issue delay data 24 indicates the delay that a sequencer needs to provide for adjusting data read commands over regulated channels from the frame buffer to allow data from the unregulated bus to be transferred over a memory read backbone. *See Frank*, col. 4, line 32-35.

In other words, Frank's data issue delay data 24 represents an artificial delay imposed on the issuance of a data read command and is not the time between issuance of a data read command and delivery of display data. Support for this position can be found throughout Frank. *See, e.g., Frank*, col. 2, line 54-56 (describing that an "adjustable delay sequencer selectively throttles data reads from the frame buffer memory so that data collisions do not occur over the memory read backbone")(emphasis added); col. 2, line 59-63 (describing that the rate at which data is obtained from the frame buffer is regulated by adjusting "the amount of delay between consecutive memory reads").

Since Frank's data issue delay is imposed to throttle consecutive memory reads, the amount of time Frank requires for a display engine to access a memory to obtain display data is this artificially imposed data issue delay. The data issue

delay is not "essentially" the latency time amount between a display data request and delivery of display data. It is a different parameter intentionally derived by Frank because unregulated operation was insufficient.

Please note that Frank's data issue delay is itself not calculated based on a latency parameter representing a latency time amount between a display data request and delivery of display data to a display buffer. In this regard, attention is respectfully directed to Frank's FIG. 3, which shows a data issue rate regulator which outputs the data issue delay data 24. *Id.*, FIG. 3; col. 2, line 31-33. The data issue rate regulator of FIG. 3 determines whether a delay is necessary based on buffer entry feedback data 18 and a threshold 28. *Id.*, col. 4, line 63-67.

Buffer entry feedback data 18 can represent the number of empty or full entries in a buffer. *Id.*, col. 3, line 18-22. Threshold 28 is a programmable threshold that controls the amount of rate regulation. *Id.*, col. 3, line 22-24. Neither of these is a latency parameter that represents a latency time amount between a display data request and delivery of display data to a display buffer, as recited in claims 1 and 29.

Wang does nothing to remedy these deficiencies in Frank. As discussed in the response filed November 28, 2006, Wang was clearly aware of latency between the memory controller accepting a request and data return. *See, e.g., Wang*, col. 2, line 36-39. However, nothing in Wang describes or suggests that parameters characterizing this latency should be determined and calculations based thereon. Any contention that it would have been obvious for one of ordinary skill to have done so represents hindsight-based reconstruction of Applicant's technology using Applicant's disclosure as a guide.

Accordingly, claims 1 and 29 are not obvious over Wang and Frank. Applicant therefore requests that the rejections of claims 1, 29, and the claims dependent therefrom be withdrawn.

CLAIM 15

Claim 15 was rejected under 35 U.S.C. § 103(a) as obvious over Wang and Frank.

Claim 15 relates to an apparatus that includes a display part which directs movement of display data, the display part including a buffer to store display data to be displayed on a display screen, and a data computing system configured to calculate one or more buffer management parameters based on a latency parameter based on a first system configuration and a buffer drain rate based on a first display mode. The latency parameter represents a latency time amount between a display

data request and delivery of display data to the buffer. The buffer drain rate represents a rate at which the display data is read from the buffer.

The rejection of claim 15 is based on the contention that Frank's data issue delay data 24 constitutes a latency parameter. Applicant respectfully disagrees and instead contends that even if Wang and Frank were combined as suggested, one of ordinary skill would not arrive at the claimed subject matter.

Like claims 1 and 29, claim 15 also explicitly recites that a "latency parameter represents a latency time amount between a display data request and delivery of display data to the buffer." As discussed above, Frank's data issue delay data 24 is not the time between a display data request and delivery and is thus not a latency parameter as recited.

Accordingly, claim 15 is not obvious over Wang and Frank. Applicant therefore requests that the rejections of claim 15 and the claims dependent therefrom be withdrawn.

CLAIM 43

Claim 43 was rejected under 35 U.S.C. § 103(a) as obvious over Wang and Frank.

Claim 43 relates to a system that includes a display, a display part which directs movement of display data to the display, the display part including a buffer to store display

data to be displayed on the display, and a data processor configured to calculate one or more buffer management parameters based on a latency parameter based on a first system configuration and a buffer drain rate based on a first display mode. The latency parameter represents a latency time amount between a display data request and delivery of display data to the buffer. The buffer drain rate represents a rate at which the display data is read from the buffer.

Just like claims 1, 15, and 29, claim 43 also explicitly recites that a "latency parameter represents a latency time amount between a display data request and delivery of display data tc the buffer." As discussed above, Frank's data issue delay data 24 is not the time between a display data request and delivery and is thus not a latency parameter as recited.

Accordingly, claim 43 is not obvious over Wang and Frank. Applicant therefore requests that the rejections of claim 43 and the claims dependent therefrom be withdrawn.

CLAIM 57

Claims 57 was rejected under 35 U.S.C. § 103(a) as obvious over Wang and Frank.

Claim 57 relates to a method of determining buffer management information for a data processing system. The method includes determining a maximum amount of time that access to a local memory to obtain data to supply a display FIFO buffer

memory may be delayed, determining a drain rate at which data is to be drained from the display FIFO buffer memory based on a display mode supported by a graphics processor, calculating a watermark value based on at least the maximum amount of time and the drain rate, and making the watermark value available for management of the display FIFO buffer memory.

Wang and Frank neither describe nor suggest elements and/or limitations recited in claim 57. For example, Wang and Frank neither describe nor suggest that a maximum amount of time that access to a local memory to obtain data to supply a display FIFO buffer memory may be delayed is determined. As discussed above, Frank's data issue delay data 24 is an artificially imposed delay. The maximum amount of time that access to a local memory to obtain data to supply a display FIFO buffer memory may be delayed in Frank is believed to include the sum of Frank's data issue delay data and a latency time between a display data request and delivery of display data.

Accordingly, claim 57 is not obvious over Wang and Frank. Applicant therefore requests that the rejection of claim 57 be withdrawn.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition,

because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Applicant asks that all claims be allowed. No fees are believed due at this time. Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: April 9, 2007

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